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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,082	09/29/2003	Jayesh R. Bhakta	NETL.001DV2	2166
20995	7590	06/24/2005	EXAMINER	
KNOBBE MARTENS OLSON & BEAR LLP			PHAM, LY D	
2040 MAIN STREET			ART UNIT	
FOURTEENTH FLOOR			PAPER NUMBER	
IRVINE, CA 92614			2827	

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	Application No. 10/674,082	Applicant(s) BHAKTA ET AL.	
	Examiner Ly D. Pham	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 April 2005.  
 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.  
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-19 is/are pending in the application.  
     4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
 6) ☒ Claim(s) 1-19 is/are rejected.  
 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
 10) ☒ The drawing(s) filed on 29 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☐ All    b) ☐ Some \*    c) ☐ None of:  
         1. ☐ Certified copies of the priority documents have been received.  
         2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
         3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
     \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>02-07-05</u> . | 6) <input type="checkbox"/> Other: _____  |

**FINAL ACTION**

**DETAILED ACTION**

1. Applicant's Information Disclosure Statement, IDS, filed February 07, 2005 has been considered by the Examiner.
2. Applicant's Terminal Disclaimer filed April 29, 2005 has been approved.
3. Applicant's Amendment filed April 29, 2005 has been entered. Claims 1, 6, 8, and 12 have been amended. New claim 19 has been added.

***Response to Arguments***

4. Applicant's arguments filed April 29, 2005 have been fully considered but they are not persuasive. Grounds for the rejection based on the amended claims set are as below.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Art Unit: 2827

6. Claims 1, 12, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Laudon et al. (US Pat 6,049,476).

Regarding **claims 1, 12, and 19**, Laudon et al. disclose a memory module comprising:

a printed circuit board—PCB (col. 1, lines 25 – 44 and col. 7, lines 6 – 14) having a first lateral portion and a second lateral portion (fig. 4, first lateral portion 110 on the left and second lateral portion 110 on the right);

a plurality of identical integrated circuits mounted in at least two rows onto at least one surface of the PCB (fig. 4, identical ICs D0 – D17 mounted on two rows 210 and 212 of one surface of module 102);

a control logic bus connected to the plurality of identical ICs (fig. 4, bus 112); and

a first register and a second register connected to the control logic bus (fig. 4, registers 214 and 216 connected to bus 112), the first register addressing the identical integrated circuits located on the first lateral portion and not addressing the identical integrated circuits located on the second lateral portion (fig. 14, register 214 addressing ICs D0 – D3 and D9 – D12 on first lateral portion 110 on the left only), and the second register addressing the identical integrated circuits located on the second lateral portion and not addressing the identical integrated circuits located on the first lateral portion (fig. 14, register 216 addressing the ICs D4 – D8 and D13 – D17 on the second lateral portion 110 on the right only).

Art Unit: 2827

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 10, 11, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laudon et al.

As per **claims 10, 11, 13, and 14**, Laudon et al. teach the first and the second register addressing the memory chips of the first row and the second row, except wherein the first register addressing the identical integrated circuits located in a first row and a second row of identical integrated circuits on a first lateral half of the at least one surface of the PCB, and the second register addressing the identical integrated circuits located in the first row and the second row of identical integrated circuits on a second lateral half of the at least one surface of the PCB; however, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to arrive at these specific features, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70.

Applicants please also note that if the disclosed parts rearrangement achieved a particular operational condition, it has also been held that where the general conditions of a claim are disclosed in the prior arts, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

9. Claims 2 – 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laudon et al. in view of Perego et al. (US Pat 6,502,161 B1).

Regarding **claims 2, 4, and 5**, Laudon et al. disclose the memory module of claim 1, except the limitations further disclosed in these claims. However, Perego et al. have taught the plurality of identical ICs comprises DDR SDRAM (col. 9, lines 41 – 46), and of types 256-Megabit or 512-Megabit (col. 3, lines 9 – 30). Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the features to the disclosure taught by Perego et al. to the disclosure by Laudon et al. so that different memory configurations can be adapted to satisfy certain system conditions (col. 3, lines 9 – 30).

As per **claim 3**, although Laudon et al. and Perego et al. did not clearly describe the limitations, in which the memory modules have an approximate dimension of 5.25 inches wide by 2.05 inches high; however, it has been held that modification involving a mere change in the size of a component is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

10. Claims 6 – 9 and 15 – 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laudon et al. in view of Yamasaki et al. (US Pat 6,594,167 B1).

Regarding **claims 6 – 9 and 15 – 18**, Laudon et al. disclose a memory module of claims 1 and 12, except wherein the identical memory ICs on the first row is 180 degrees in orientation with the identical memory ICs on the second row. However, this feature has been taught by Yamasaki et al. (fig. 19).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to include the feature shown by Yamasaki to the disclosure by Laudon et al. so that each memory chip data I/O pin is nearest to center line to achieve equidistance—timing optimization (col. 11, line 43 – col. 12, line 2).

### ***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

13. When responding to the office action, Applicant(s) are advised to provide the examiner with the page and line numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly Pham   
June 20, 2005

  
HOAI HO  
PRIMARY EXAMINER